Double Balanced Mixers Using Active and Passive Techniques

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Abstract—**A variety of double balanced mixers, employing dual-gate FET's or diodes as the mixing nonlinearities, have been fabricated using planar monolithic circuit technology. The mixer topologies, which use active balancing methods, eliminate the need for large suspended substrate structures, thus minimizing circuit area and facilitating integration. These unique approaches also eliminate IF extraction problems and combine the best performance characteristics of FET's and diodes.**

I. Introduction

TRADITIONALLY, the mixer has been the most difficult element to design and analyze in modern microwave receiver systems. The vast majority of these systems employ passive diode mixers as the state-of-the-art frequency converting element, but active FET implementations are beginning to appear. These mixers typically employ large transmission line baluns used in three-dimensional structures, although completely planar 2–18 GHz double balanced mixers have been demonstrated [1]–[3]. Conventional mixer designs such as these are not feasible for monolithic implementation since their passive elements require excessive GaAs area. Hence, a completely new design concept must be used in the development of GaAs monolithic microwave mixers.

II. General Mixer Operation

The mixer, which can consist of any device capable of exhibiting nonlinear performance, is essentially a multiplier. That is, if at least two signals are present, their product will be produced at the output of the mixer. This concept is illustrated in Fig. 1. The RF signal applied has a carrier frequency of ω_s with modulation $A(t)$, and the local oscillator signal (LO or pump) applied has a pure sinusoidal frequency of ω_p. From basic trigonometry, we know that the product of two sinusoids produces a sum and a difference frequency. Either of these frequencies can be selected with the IF filter. Unfortunately, no physical nonlinear device is a perfect multiplier. Thus, they contribute noise and produce a vast number of spurious frequency components. If the small-signal case is assumed and modulation is ignored, the mixer output spectra can be defined as

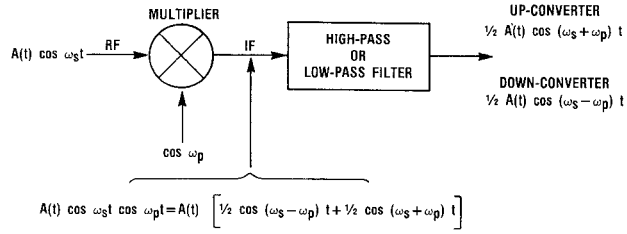

Fig. 1. Ideal multiplier mixer model showing both up- and down-converter performance.

$$\omega_d = n\omega_p \pm \omega_s. \tag{1}$$

The desired component is usually the difference frequency ($|\omega_p + \omega_s|$; or $|f_p - f_s|$), but sometimes the sum frequency ($f_s + f_p$) is desired when building an up-converter or a product related to a harmonic of the LO, as in a subharmonically pumped mixer.

A mixer can also be analyzed as a switch which is commutated at a frequency equal to the pump frequency ω_p. This is a good first-order approximation of the mixing process for a diode (or a FET) since it is driven from the low-resistance state (forward bias) to the high-resistance state (reverse bias) by a high-level LO signal. The simplified diode switching model is shown in Fig. 2. With this switching action in mind, a single-ended mixer can be represented by the circuit in Fig. 3(a). In this example the RF signal appearing at the IF load is interrupted by the switching action of the diode which is caused by the pump. From the modulation theorem, it can be shown that the sum and difference frequencies appear at the IF port as well as many other products. It should be remembered that a dc component is also present and must not be suppressed in a physical diode mixer if proper operation is to be obtained. The circuit shown in Fig. 3(b) is equivalent to a double balanced mixer. In this instance, the time average of the RF signal and LO dc component does not appear at the IF port. Since there is no LO dc component in the LO waveform, there is no switching product at the LO port with a frequency component of the fundamental RF signal. Hence, the mixer also has LO to RF port isolation without requiring filters, as in the single-ended case.

Recently, the growing interest in GaAs monolithic circuts is again beginning to heighten the interest in active

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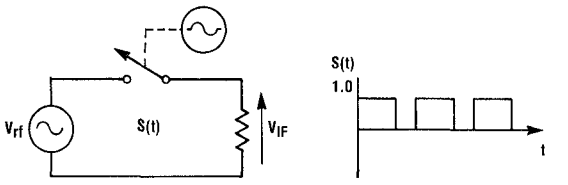


Fig. 2. Single-ended mixer employing diode switching model.

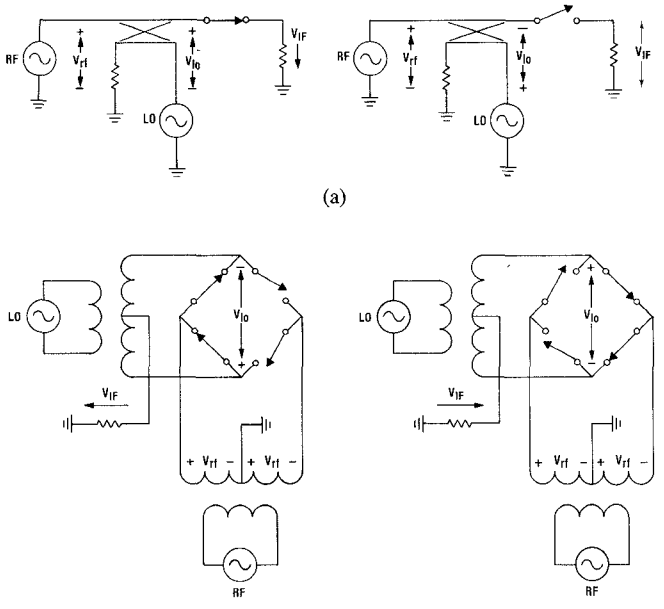


Fig. 3. Typical mixer circuits employing diode switching model depicting IF voltage (or current) as a function of LO polarity. (a) Single-ended mixer. (b) Double balanced mixer.

MESFET mixers. This is indeed fortunate, since properly designed FET mixers offer some distinct advantages over their passive counterparts. This is especially true in the case of the dual-gate FET mixer. Since the additional port allows for some inherent LO to RF isolation, it can at times replace single balanced passive approaches. The possibility of conversion gain rather than loss is also an advantage, since the added gain may eliminate the need for excess amplification, thus reducing system complexity.

There are several drawbacks when designing active mixers. With diode mixers, the design engineer can make excellent first-order performance approximations with linear analysis and is given the practical reality that a diode always mixes reasonably well almost independently of the circuit. These conditions unfortunately do not hold for active mixer design. Simulating performance, especially with a dual-gate device, requires some form of nonlinear analysis tool if any circuit information, other than small-signal impedance, is desired. An analysis of the noise performance is even more difficult.

The dominant nonlinearity of the FET is its transconductance [5]–[7], which typically, especially with JFET's, is a square-law function. Hence, it makes a very efficient multiplier with reasonably low spurious products. The small-signal circuit shown in Fig. 4 denotes the principal

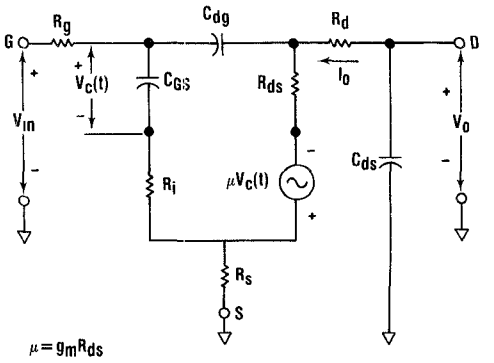


Fig. 4. Small-signal GaAs FET equivalent circuit with voltage source representation.

elements of the FET that must be considered in a FET model [4]. The parasitic resistances R_g, R_d, and R_s are small compared to R_{ds} and can be considered constant, but, they are important in determining the noise performance of the circuit. The mixing products produced by parametric pumping of the capacitances C_{gs}, C_{dg}, and C_{ds} are typically small and only add second-order effects to the total circuit performance. Time-averaged values of these capacitances can be used in circuit simulation with good results.

This leaves the FET transconductance g_m, which exhibits an extremely strong nonlinear dependence as a function of gate bias. A typical transconductance versus gate bias for a 150 μm low-noise FET is shown in Fig. 5. It is evident from this illustration that the greatest percentage change in transconductance occurs near pinch-off, with the most linear change with respect to gate voltage occurring in the center of the bias range. As the FET is biased toward I_{dss}, the transconductance function again becomes nonlinear. It is in these most nonlinear regions that the FET is most efficient as a mixer.

Single-ended, as well as balanced, mixers can also be designed using dual-gate FET's [8], [9]. Dual-gate devices offer several advantages over conventional devices, such as ease of LO injection, improved isolation, and added gain. However, they are considerably less stable, and hence added care must be used when designing such circuits.

The operation of a dual-gate FET can be easily understood if the FET is considered as a cascode connected FET pair. Using this concept for the FET, the drain characteristics for the pair can be approximated by combining the characteristics of each intrinsic FET. This concept is illustrated in Fig. 6(a). A slightly more convenient representation of the drain characteristics is shown in Fig. 6(b). With this representation the operating point for FET 1 can be found as a function of gate 1 and gate 2 bias as well as its drain-to-source voltage.

The operating point can vary significantly depending on how the FET is biased. Typically, gate 1 is used for signal injection with gate 2 biased ($V_{gs2} < 0$) for FET operation in the low-noise mode (shaded area in Fig. 6(b)). Gate 2 is also used for LO injection. Applying the LO at gate two is in effect drain pumping the first FET; hence, FET

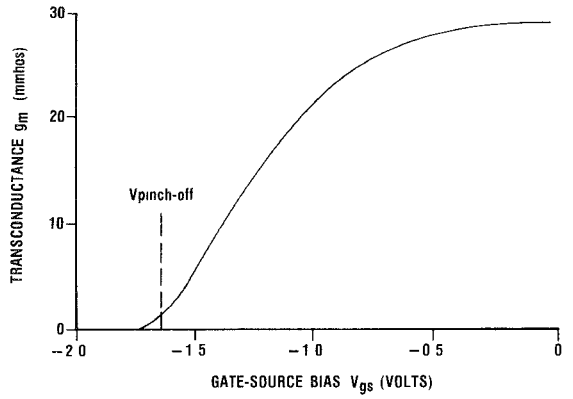
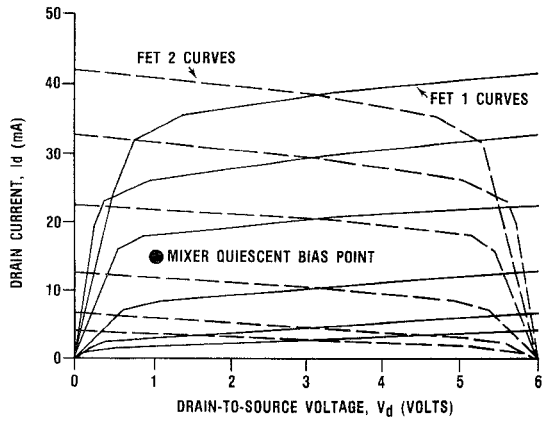
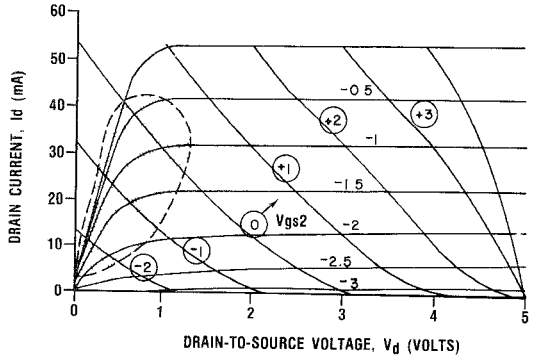


Fig. 5. Transconductance, as a function of gate bias, for a typical 150-μm-gate-width FET.



(a)



(b)

Fig. 6. Dual-gate FET I–V characteristics. (a) Intrinsic FET I–V characteristics connected "back-to-back" to simulate a dual-gate FET. (b) Dual-gate FET I–V characteristics as a function of V_{gs1} and V_{gs2}.

1 is the primary mixing element. The operation is reversed if a sufficiently high bias voltage ($V_{gs2} > 2$) is applied to gate 2. With these bias conditions, FET 1 acts as an RF preamplifier while FET 2 becomes the primary mixing element.

Slightly more insight into the operation of a dual-gate FET mixer can be had by examining the drain current dependence due to gate 1 and gate 2 bias voltage (Fig. 7) and the conversion gain characteristics as a function of LO drive voltage as reported by Tsironis [10], [11] (Fig.

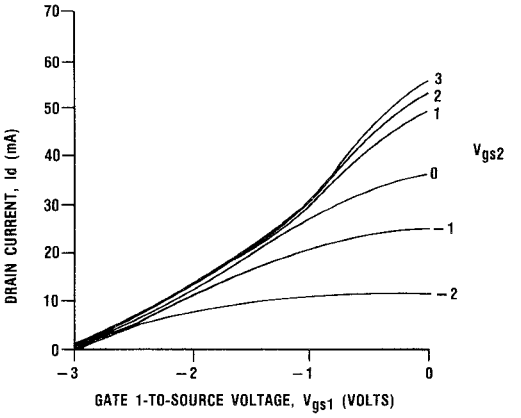


Fig. 7. Dual-gate FET drain current as a function of V_{gs1} and V_{gs2}.

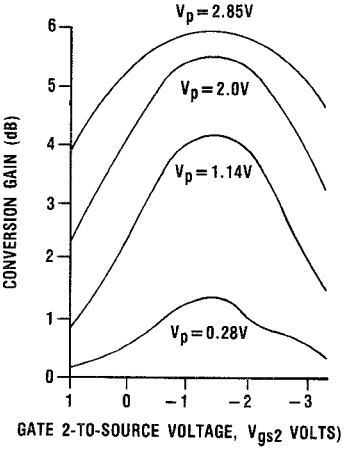


Fig. 8. Conversion gain characteristics of dual-gate FET as a function of LO peak voltage.

8). As can be seen, a large percentage change in drain current, as a function of gate bias, occurs in both of the operating regions described above; hence, maximum conversion gain should also correspond to the same operating points. Also, as in the case of the single-gate mixer, the conversion gain increases as the LO drive voltage is increased until the point of LO saturation.

Dual-gate FET mixers can be analyzed with the aid of a nonlinear simulator such as Microwave HARMONICA, LIBRA, or Microwave SPICE. Conversion performance obtainable with dual-gate mixers is comparable to that obtained with conventional devices [7], [10], with the exception of slightly degraded noise figure and possibly more gain. There is also some indication that the intermodulation performance for dual-gate MESFET devices may be better than that of single-gate FET's; but this idea has not yet been proven.

Unfortunately, the best mixer conversion loss is obtained for large values of LO voltage. With this in mind, and knowing the FET parasitic element values, which can be obtained from small-signal S-parameter measurements, an estimate of the required LO can be made. From conventional circuit theory, the power dissipated in the gate circuit is

$$P_{LO} = 0.5(\omega_p \tilde{C}_p V_p)^2 R_{in} \qquad (2)$$

where R_{in} is the input resistance, $\tilde{C}_p$ is the time-averaged value of C_{gs}, and V_p is the pinch-off voltage. When the total gate periphery of the FET is small, the optimum LO power will be modest (3 to 6 dBm), but as the FET becomes larger, the term $\tilde{C}_p$ in (2) begins to dominate. It is not uncommon for a large FET to require 20 dBm of LO drive power. The amount of LO power required for maximum conversion loss with a particular FET size can also be reduced by selecting or designing the FET for the lowest possible value of pinch-off voltage. For a given gate periphery, the values of R_{in} and C_p change little compared to the change in the pinch-off voltage obtained when changing the FET doping profile. Thus, a dramatic improvement in LO efficiency is obtained when using low-noise FET's with pinch-off voltages in the 1.5 V range as compared to power FET's that exhibit pinch-off voltages in the 4 to 5 V range. Experimental results, for both single and multiple FET mixers, verify the above predictions for optimum conversion loss, bias, and LO requirements [6].

The noise performance of a GaAs FET mixer is much less understood than its companion amplifier. However, the noise figure performance is related to the intrinsic noise sources of the FET (R_g, R_s, and R_d) as well as to shot noise and noise due to traps in the semiconductor material. The $1/f$ noise spectra of the GaAs FET mixer can extend to several hundred MHz, but usually, with a well-designed FET, extends to less than 50 MHz. A variety of single-gate mixers, with operating frequencies extending through X-band, have been reported to exhibit noise figures less than 5 dB with an associated gain of several dB. This performance, although not easy to realize, is quite comparable to conventional diode mixers, except that a small amount of gain, not loss, is obtained. However, a good first-order approximation to the noise figure performance of a single-gate FET mixer can be determined by applying the accepted noise parameters for MESFET's [12].

III. Monolithic Mixer Design

The design problem for any type of mixer can be divided into two main areas: the nonlinear element and the balun. If a monolithic implementation is desired, the most practical choices for nonlinear elements are planar Schottky diodes, single-gate FET's, and dual-gate FET's.

In the monolithic realm, the balun problem is further constrained by chip area and backside processing requirements. If a 2 to 18 GHz passive mixer balun were used, it would be approximately 2 cm in length, which is an order of magnitude too large for a monolithic circuit realization. Thus, active baluns or lumped element transforms are the only viable options. The problem is further complicated in that it is desirable to employ baluns that approximate low-frequency equivalent center-tapped transformers. A center-tapped balun is a convenient way to extract the IF frequency from a conventional double balanced diode mixer. However, a center-tapped transmission line balun cannot be fabricated.

A new balun topology, which can be readily implemented using monolithic technology, has been devised that eliminates the above problems and provides a virtual center tap. Since the balun uses common-gate and common-source circuit techniques, an ideal 180° phase shift occurs for the signals present between the upper and lower halves of the circuit (Fig. 9). Typical broad-band amplitude and phase performance for a balun designed with no center tap and resistive terminations at the reverse end of the drain transmission line is shown in Fig. 10(a) and (b). The balun shown in Fig. 10(c) measures 1.87 by 1.73 mm. As can be seen, the balun exhibits excellent balance through the design band of 2–18 GHz. The performance of a center-tapped balun designed for the same frequency range is shown in Fig. 11. The performance is slightly degraded due to the removal of the drain terminations.

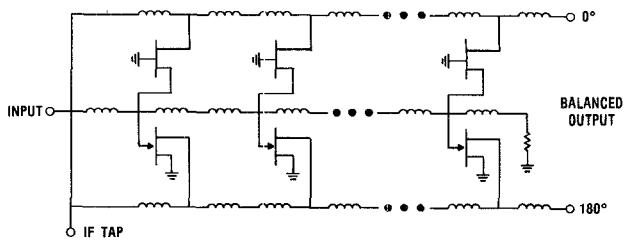


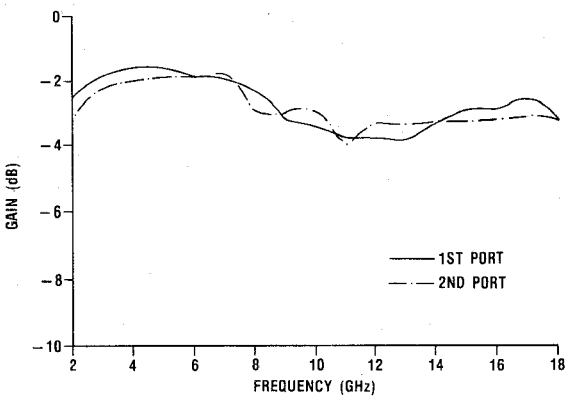
Fig. 9. Lumped element equivalent circuit of center-tapped balun.

If two such baluns are used in conjunction with a diode or FET ring to form a double balanced mixer, the IF signal appearing at the ring terminals propagates (in phase) down both arms of the balun and can be summed at a common node, thus forming a virtual center tap. This center tap can be used for IF extraction or grounded to complete the IF return path. Since active baluns are not reciprocal, a combining or dividing structure will be needed on the RF port, depending on whether the mixer is used as a up- or down-converter (Fig. 12).

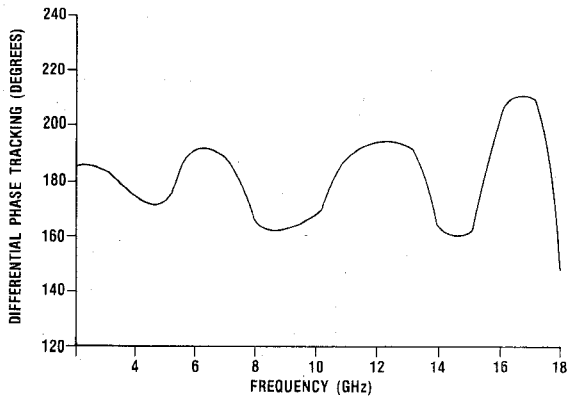
The frequency limitations of the RF and LO ports are determined by the distributed-amplifier-like sections, which can be designed to operate over extremely large bandwidths. The IF frequency response can also be designed to exhibit broad-band performance. This mixer concept can also be extended to include double-ring mixer topologies (Fig. 13). Double-ring approaches have the added advantage of allowing the IF frequency response to overlap the RF and LO frequency bands, thus making IF extraction even easier.

By using the above-mentioned technology, both single- and double-ring designs of the types depicted in Figs. 12(a) and 13 were fabricated. The conversion loss characteristic, at an IF frequency of 4 GHz of a typical single-ring down-converter, is shown in Fig. 14. As can be seen in the above illustration, the performance is comparable to that of conventional diode designs requiring similar amounts of pump power (12 dBm). With the LO drive shown, the mixer exhibited a 1 dB compression point (referred to the input) of 4 dBm (Fig. 15), LO to RF isolation of 20 dB (average), LO to IF isolation of 30 dB (average), and RF to IF isolation greater than 20 dB (Fig. 16).

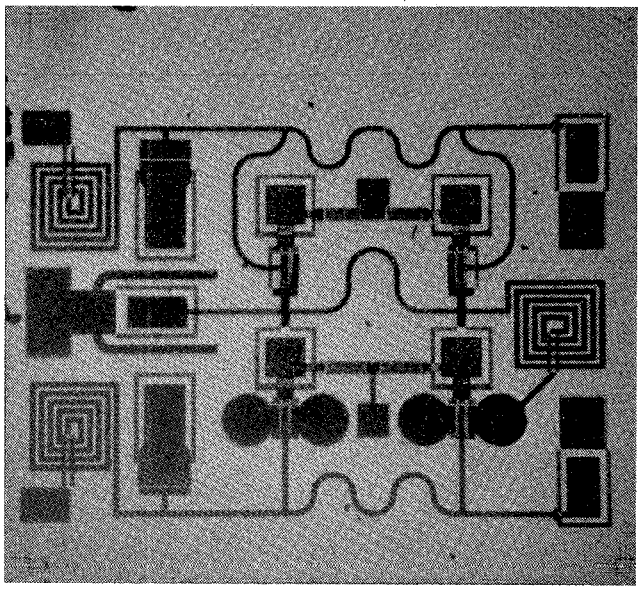
The conversion performance as a function of fre-



(a)



(b)



(c)

Fig. 10. Monolithic balun performance. (a) Frequency response and amplitude balance. (b) Differential phase performance. (c) Chip photograph.

quency, which was measured at an IF frequency of 500 MHz, for the double-double balanced design is shown in Fig. 17. Although the mixers employ diodes as the nonlinear element, the conversion loss (gain) of the double-ring design is somewhat greater than that of a conventional structure because of the gain associated with baluns. The isolation characteristics, which are comparable

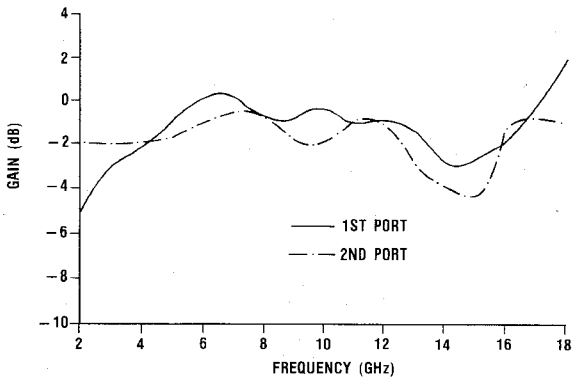
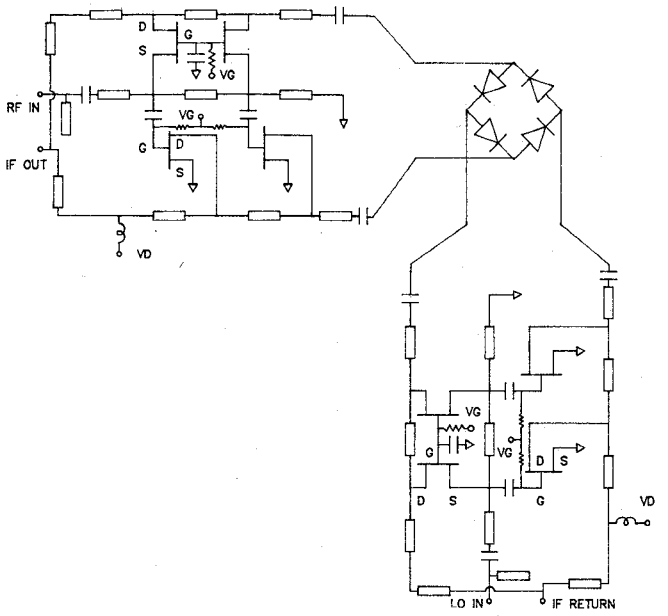
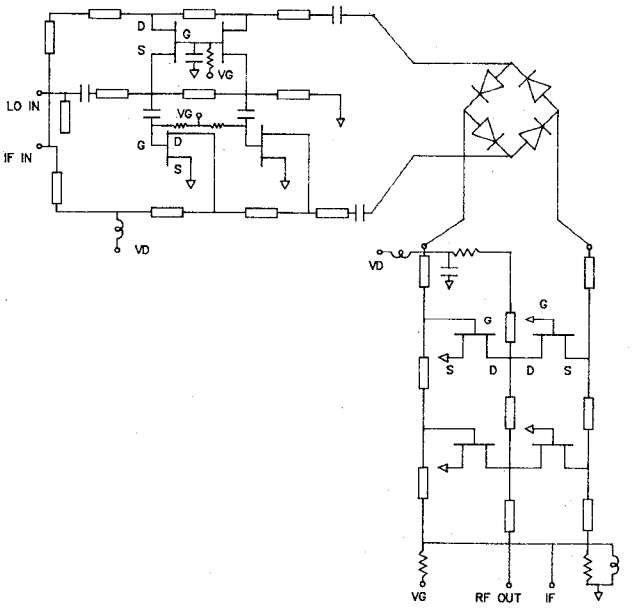


Fig. 11. Center-tapped balun performance.



(a)



(b)

Fig. 12. Active balun diode mixers. (a) Down-converter mixer circuit diagram. (b) Up-converter mixer circuit diagram.

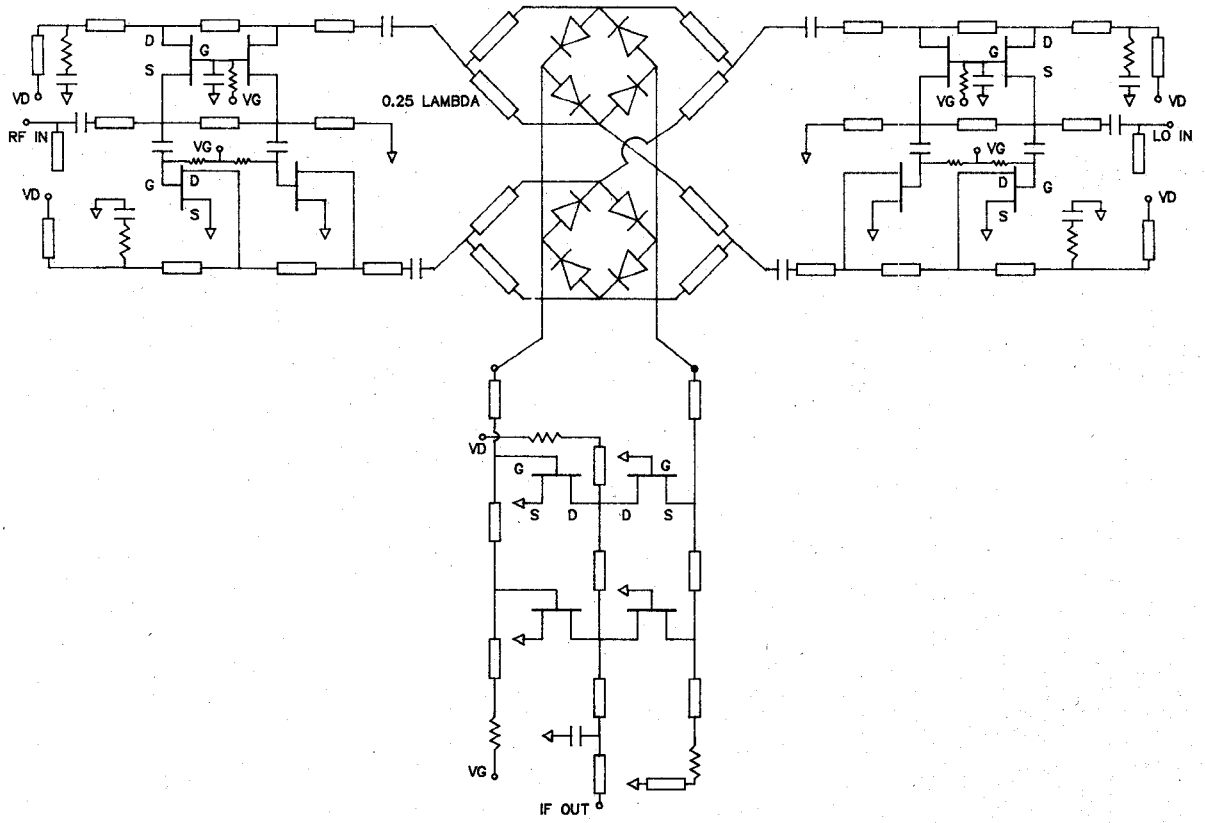
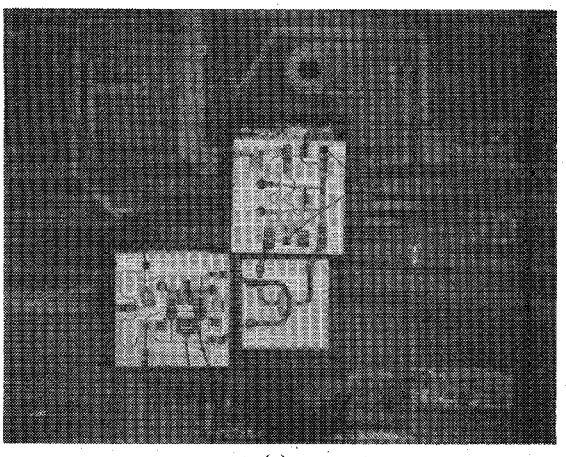
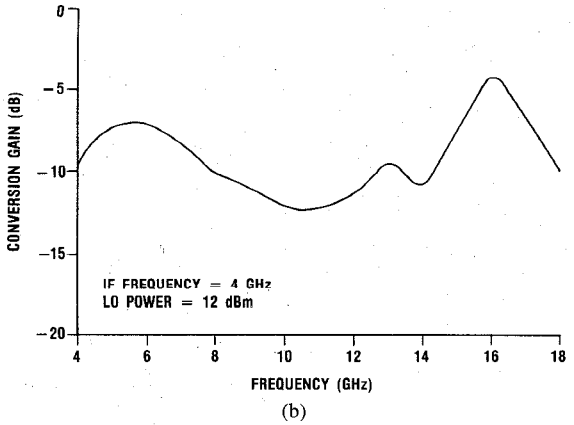


Fig. 13. Circuit diagram of double-ring mixer.



(a)



(b)

Fig. 14. Monolithic double balanced diode mixer. (a) MMIC photograph. (b) Conversion loss performance of down-converter mixer.

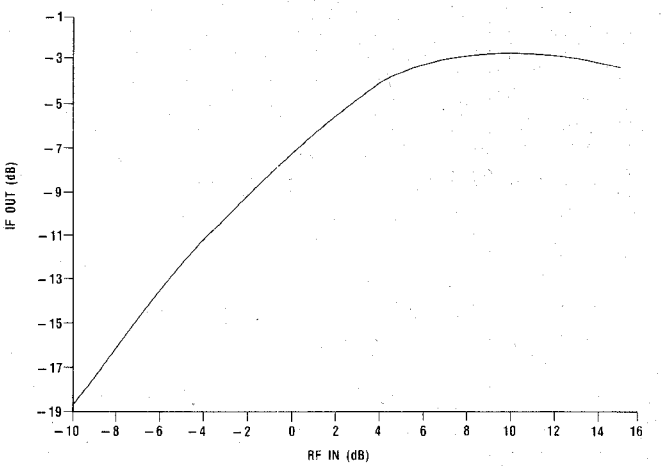


Fig. 15. RF compression characteristics of double balanced monolithic diode mixer.

to hybrid designs, are shown in Fig. 18. The compression characteristics of this configuration measured with conventional levels of LO drive (13 dBm) is shown in Fig. 19. As can be seen, the mixer exhibited a 1 dB compression point (referred to the input) of 8 dBm, which is comparable to the best hybrid designs.

A slightly different topology that can be readily implemented using monolithic technology employs active baluns in conjunction with a unique distributed dual-gate FET mixer structure. The proposed circuit employs a single balun, which can be of either the active or the passive lumped element type (transformer, differential line, etc.), and distributed dual-gate FET mixer sections. Transmis-

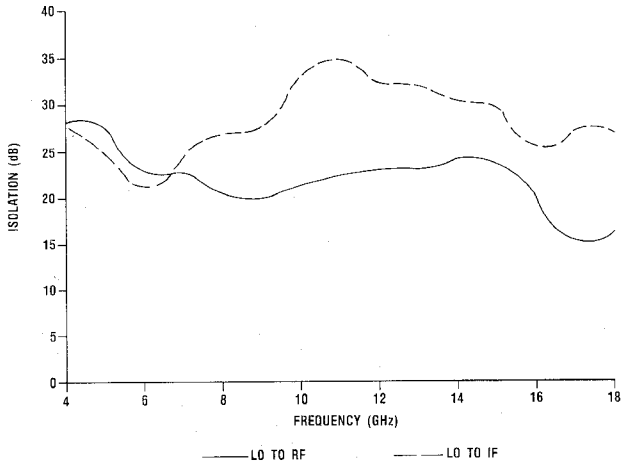
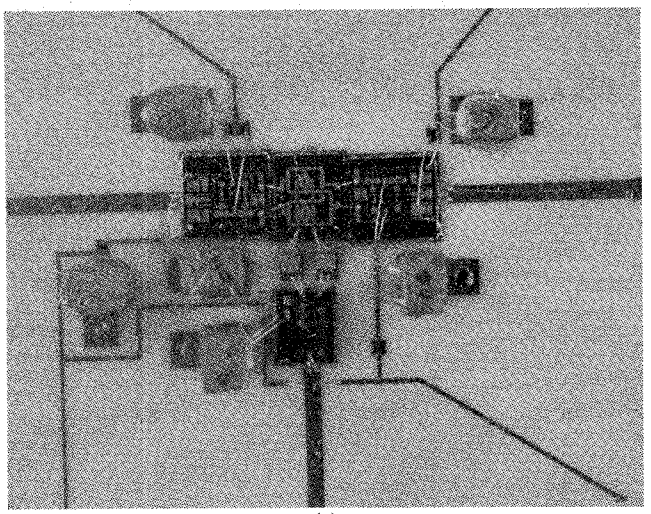
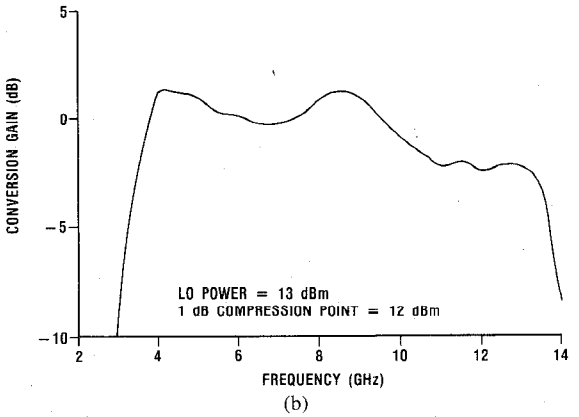


Fig. 16. Isolation characteristics of double balanced monolithic diode mixer.



(a)



(b)

Fig. 17. Monolithic double ring mixer. (a) Chip photograph. (b) Conversion loss performance.

sion line models for the balun and mixer are shown in Fig. 20. The number of distributed sections employed depends on the bandwidth, conversion gain, and impedance matching requirements. In the above design only two sections were required to achieve adequate distributed performance. However, greater conversion gain could have

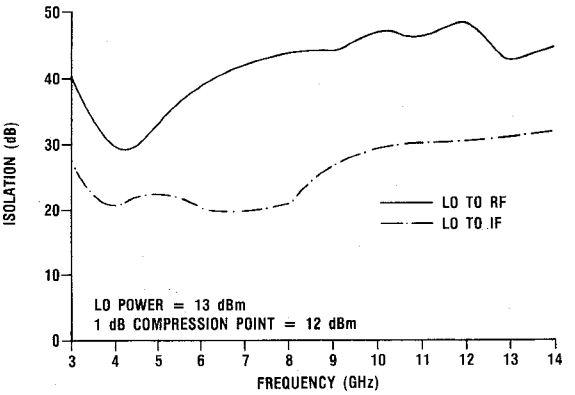


Fig. 18. Isolation performance of monolithic double-ring mixer.

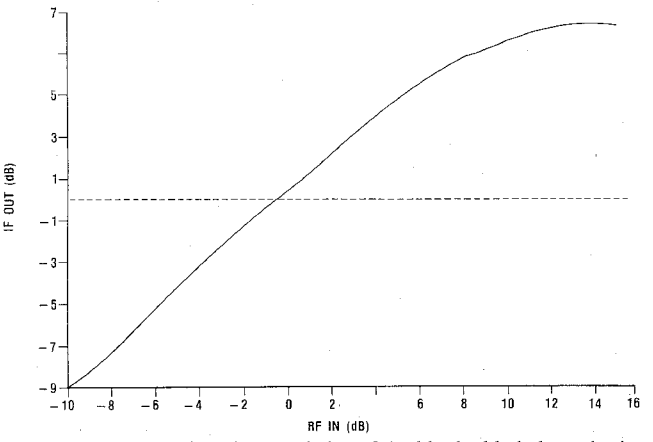


Fig. 19. RF compression characteristics of double double balanced mixer.

probably been obtained if more sections were employed at the expense of chip complexity.

As can be seen in the circuit diagram, one mixer section employs a common-source topology while the other uses a common-gate topology; these are inherently antiphase. Thus, as ideal 180° phase shift occurs for the signals present between the upper and the lower half of the circuit, eliminating the requirement for second balun. Both the LO and RF voltages, which are present at the FET drains of each mixer section, are also out of phase by 180° while the IF voltages are in phase. By summing the output of both mixer sections, an independent IF port is obtained and the RF and LO signals are canceled. Thus, the mixer structure is completely double balanced.

The frequency limitations of the mixing portion of the circuit are determined by the distributed-amplifier-like sections, which can be designed to operate over extremely large bandwidths. With the addition of an IF amplifier (active matching) or bandpass matching network, the IF frequency response could also be further broadened. Because of the large number of active nonlinear elements, the dynamic range can be made as good as or better than the best conventional diode mixers.

The distributed monolithic balun and mixer shown in Fig. 21 was designed using 0.5 μm × 150 μm dual-gate FET's fabricated on a 0.15-mm-thick GaAs substrate. The FET's were modeled as cascode connected single-gate FET's with the linear model elements determined from *S*-

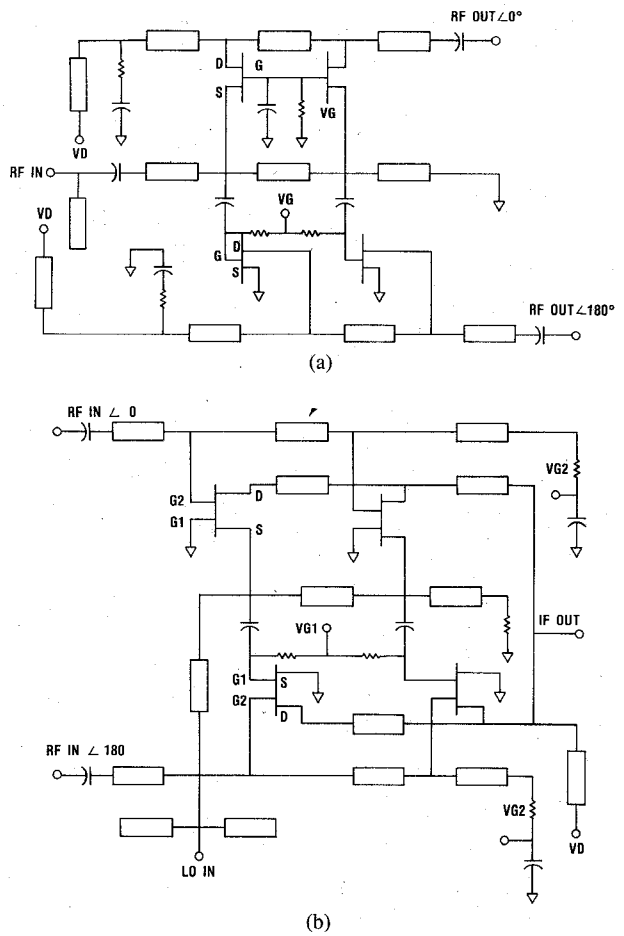


Fig. 20. Dual-gate FET double balanced mixer. (a) Transmission line model of distributed active balun. (b) Transmission line model of monolithic mixer chip.

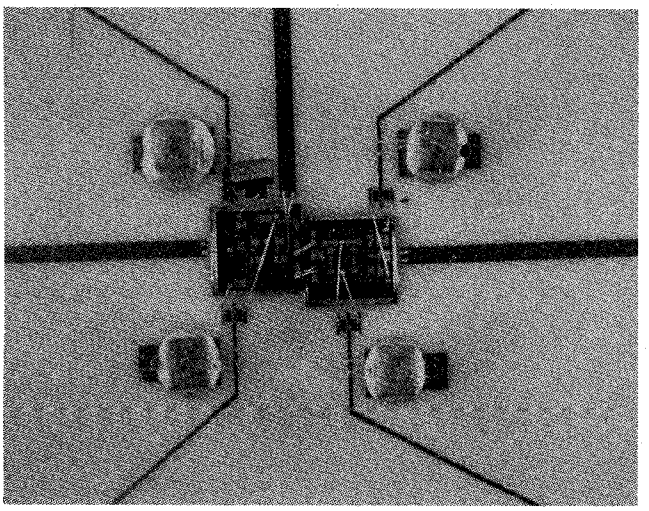


Fig. 21. Monolithic double balanced mixer and active balun IC's.

parameter measurements. The nonlinear drain current and transconductance characteristics were obtained from I–V curve data obtained at 1 mHz [13] and are shown in Fig. 6(a). The active balun used with the mixer also employed both distributed common-source and common-gate amplifier sections in order to obtain a broad-band differential phase output with good amplitude balance.

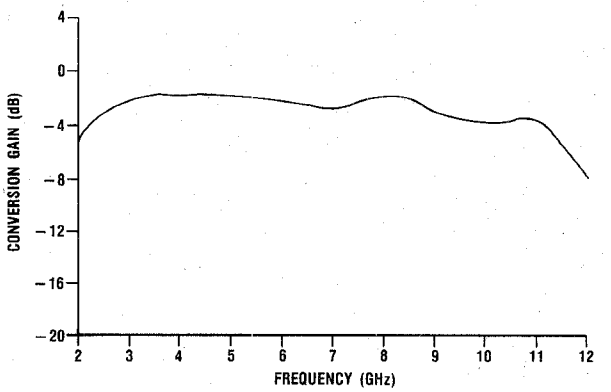


Fig. 22. Monolithic double balanced FET mixer conversion loss performance as a function of frequency.

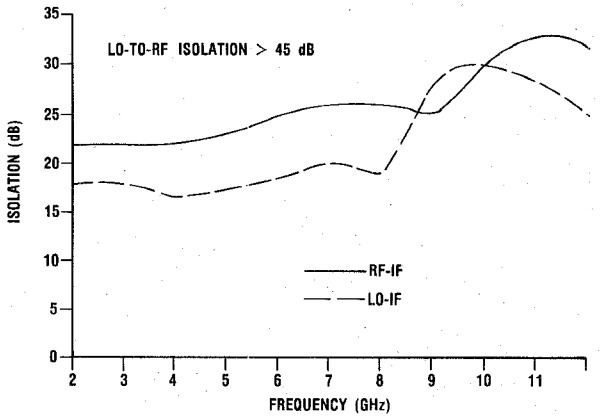


Fig. 23. Isolation performance of double balanced FET mixer.

The mixer/balun combination was evaluated as a conventional double balanced mixer with the LO drive applied to the gate 1 circuit. The RF signal was applied to the active balun, which in turn drives the gate 2 circuit. The dc bias on both gates was adjusted for optimum conversion loss. However, since the mixer performance was very insensitive to bias, the second gate voltage was set to zero while the first gate was biased for a drain current of $I_{dss}/2$. Using the above bias conditions, the conversion loss characteristic shown in Fig. 22 was obtained. The RF to IF and LO to IF isolations, which demonstrate the excellent balance obtained in the design, are shown in Fig. 23. Conversion loss performance as a function of LO power and the RF compression characteristics are shown in Figs. 24 and 25. As can be seen, the mixer's performance is comparable to that of hybrid diode designs.

This type of structure, with its unique balanced characteristics, can be used as a broad-band up-converter as well as a conventional mixer in a variety of receiver applications. In addition, since the mixer is completely balanced, the IF frequency response can overlap the LO or RF responses, which usually can only be accomplished with double-double balanced structures.

IV. Mixer Fabrication

Fabrication of the above balun and mixer structures was accomplished by using a Texas Instruments (TI) baseline ion-implanted GaAs process for 3-in-diameter, 0.15-mm-

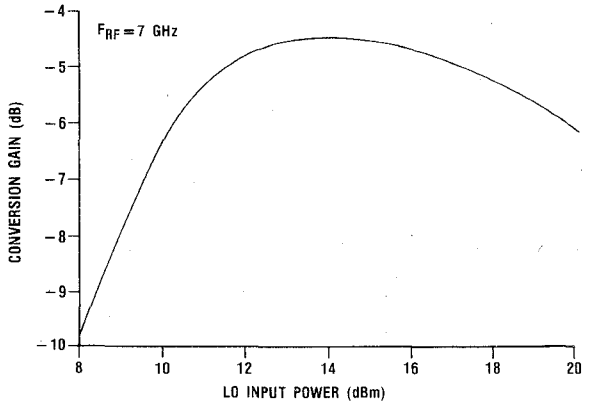


Fig. 24. Conversion loss as a function of LO power.

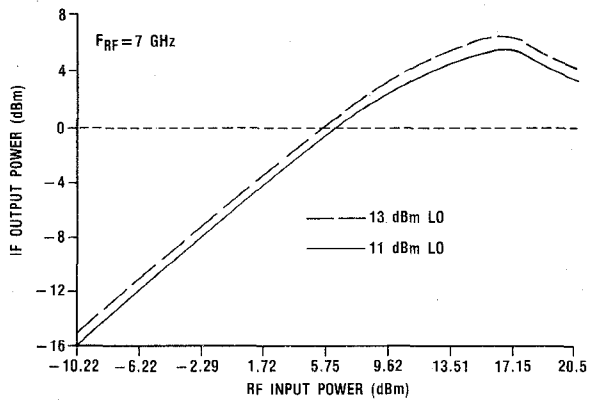


Fig. 25. RF compression characteristics of double balanced dual-gate FET mixer.

thick semiconductor wafers. The FET channel doping profile was optimized for high transconductance and low-noise performance yielding the best mixer performance. The TiPtAu 0.5 μm gates were defined with E-beam lithography, the ohmic metal employed was AuGeNiAu, and the MIM (metal–insulator–metal) capacitors were constructed with a 2000-Å-thick layer of Si_3N_4. The same baseline low-noise FET process was also used to fabricate the diode structures.

V. Conclusion

By using this dual-mode characteristic of distributed broad-band baluns in diode mixer topologies, a very compact monolithic circuit can be designed to operate over a frequency range several octaves wide with performance comparable to that of conventional passive diode mixers. An alternate all-FET structure with its unique balanced characteristics can also be used as a broad-band up-converter as well as a conventional down-converting mixer in a variety of receiver applications. Since this mixer is completely balanced, the IF frequency response can overlap the LO or RF responses, which usually can only be accomplished with double-double balanced structures.

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*

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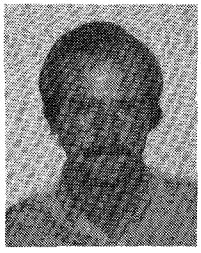
Dr. Pavio's overall design experience includes broad-band microwave components, including mixers, oscillators, hybrids, stripline arrays, monopulse feeds, traveling-wave amplifiers, waveguide antennas, microwave amplifiers, and stripline/coaxial filters. He also holds more than ten patents and has published more than 40 technical publications in the areas of
monolithic circuit design, electromagnetic analysis, and nonlinear modeling.



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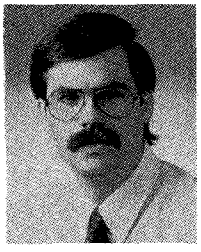

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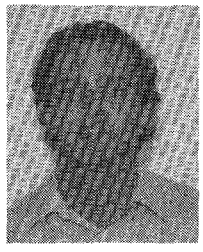

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That same year he joined Texas Instruments, where he is currently assigned to the Electronic Warfare Component Development entity as a Microwave Design Engineer responsible for the receiver/limiter portion of a MMIC generic decoy, for which he designed and developed a wide-band MMIC mixer. Previous assignments included the design and development of a monolithic wide-band MMIC power amplifier.

Mr. Sapashe is a member of Tau Beta Pi and Phi Kappa Phi.